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10/773,673	02/06/2004	Gerald George Pechanek	800.0141	7530

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,673	PECHANEK ET AL.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 9-26 have been examined; Claims 1-8 have been cancelled.

Acknowledgment of papers filed: appeal briefs filed on 9, 24 and 28 of April 2008. The papers filed have been placed on record.

Specification

2. The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9 and 18-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheaffer (U.S. Patent No. 6,957,321) in view of Miller (U.S. Patent No. 6,847,365).

5. Regarding claim 9, Sheaffer discloses a very long instruction word memory system (col 5 lines 48-51) comprising: a memory having a plurality of instruction slots for storing instruction words at addressable locations in the memory from which instructions may be fetched for execution (col 7 lines 1-3); said plurality of instruction slots comprising at least expanded width instruction slot having a width that is greater

than the standard width instruction slots, the expanded with instruction slot used for storing an expanded width instruction having a format that is wider than the standard with instructions (col 1 lines 33-50 or col 2 line 65 to col 3 line 7);

The VLIW memory configured for loading said at least one expanded format slot with an expanded instruction (col 7 lines 1-3).

Sheaffer fails to disclose that VLIW memory and a standard size VLIW instruction.

Miller discloses a VLIW system with variable length VLIW instructions (col 13 lines 1-4)

Sheaffer would have been motivated to utilize this more massively VLIW approach in order to maximize efficiency of the processing units "so that for every clock cycle, each processing unit may execute a separate instruction."

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Sheaffer and incorporate the variable length VLIW instructions of Miller. The combination would still incorporate the functionality of Sheaffer in that Sheaffer is capable of combining two microinstructions (a normal instruction and a NOP) of the VLIW instruction for expanded operand capabilities.

6. Regarding claim 18, Sheaffer/Miller discloses a very long instruction word (VLIW) memory system (col 5 lines 48-51) comprising: an instruction memory holding a plurality of instructions of a first bit width , the plurality of instructions having at least one execute VLIW instruction (Miller col 13 lines 1-4); and a very long instruction memory having

instruction slots for storing instructions of a second bit width different from the first bit width and wherein the very long instruction memory holds VLIWs at addressable locations that may be fetched as a result of executing the at least one execute VLIW instruction (col 1 lines 33-50 or col 2 line 65 to col 3 line 7 and Miller col 13 lines 1-4).

7. Regarding claim 19, Sheaffer/Miller discloses the system of claim 18 wherein instructions of the second bit width are stored in a data memory and delivered to the very long instruction memory utilizing a data bus (col 5 lines 48-51 and col 7 lines 1-3 and fig 4 reference 410 and Miller col 13 lines 1-4).

8. Regarding claim 20, Sheaffer/Miller discloses a very long instruction word (VLIW) memory system (Miller col 13 lines 1-4) comprising: a plurality of instruction slots for storing instruction words forming a VLIW (Miller col 13 lines 1-4), at least one of said plurality of instruction slots having a compressed format for storing a compressed instruction having a narrower instruction format with respect to an instruction format required in a program storage wherein the VLIW resides at an addressable location in a VLIW memory, the VLIW memory holding VLIWs that may be fetched for execution (col 1 lines 33-50 or col 2 line 65 to col 3 line 7 and Miller col 13 lines 1-4);

Note that on paragraph 53 of Applicant's specification, the instructions designated as "compressed instructions" appear to be essentially the same as the extended instructions, just through a different view point. As claimed (in light of the

Applicant's specification), it appears reasonable to consider the non-extended instruction a compressed instruction.

And means for loading said at least one compressed format slot with a compressed instruction (Miller col 13 lines 1-4)

9. Regarding claim 21, Sheaffer/Miller discloses a processing apparatus comprising: a memory for storing a processing apparatus program comprising short instruction words (col 7 lines 1-3); an indirect very long instruction word (VLIW) memory comprising a plurality of instruction slots for storing instruction words (col 5 lines 48-51 and col 7 lines 1-3 and Miller col 13 lines 1-4),

Note that the term "indirect" appears to be referring to an "indirect execution mechanism" in Applicant's specification. This mechanism is anticipated by the additional NOP operands that are indirectly used in execution.

At least one of said instruction slots having an instruction format sized according to execution function and operand storage capacity (col 3 lines 1-7)

And independent of the size of the short instruction words , wherein the plurality of instruction slots are organized to form a plurality of VLIWs and each VLIW resides at an addressable location in the indirect VLIW memory, the indirect VLIW memory holding VLIWs that may be fetched for execution (col 3 lines 1-7);

At least one data memory unit storing instruction operands (fig 4); and at least two execution units for executing a VLIW fetched from the indirect VLIW memory (col 6

lines 35-36 and Miller col 13 lines 1-4) in response to a short instruction word dispatched from the memory (see below).

10. Regarding claim 22, Sheaffer/Miller discloses the processing apparatus of claim 21 wherein the short instruction words comprise K-bits (fig 5) and the instruction format comprises T-bits, wherein T.noteq.K (col 3 lines 1-7).

11. Regarding claim 23, Sheaffer/Miller discloses the processing apparatus of claim 22 wherein the instruction format comprises at least one operand address field of B-bits supporting direct operand addressing (fig 4a reference 515).

12. Regarding claim 24, Sheaffer/Miller discloses the processing apparatus of claim 23 wherein the data memory unit has a capacity 2.sup.B data values (see below).

Note that it is clearly implied that there are 2^B data values. That is the whole point of having B bits in an address.

13. Regarding claim 25, Sheaffer/Miller discloses the processing apparatus of claim 21 wherein a at least one of the at least two execution units operate on a slot instruction format and directly access operands from the data memory unit for execution (fig 5 and col 3 lines 1-7).

14. Regarding claim 26, Sheaffer/Miller discloses the processing apparatus of claim 21 wherein the at least two execution units operate as two execution units (col 6 lines 35-36)

When executing two VLIW memory slot instructions as specified by a two slot execute VLIW instruction (fig 5 and col 5 lines 49-51 and Miller col 13 lines 1-4),

And wherein the at least two execution units operate as one execution unit when executing one VLIW memory slot instruction as specified by a one slot execute VLIW instruction (col 3 lines 1-7).

15. Claims 10, 11, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheaffer/Miller in view of Moller (U.S. Patent No. 6,826,522).

16. Regarding claim 10, Sheaffer discloses the memory system of claim 9 wherein the plurality of instruction slots comprise a store unit instruction slot (col 9 lines 13-19), a load unit instruction slot (col 9 lines 13-19),

An arithmetic logic unit (ALU) instruction slot (col 9 lines 14-15), and a data store unit (DSU) instruction slot (col 9 lines 13-19).

Sheaffer/Miller fails to disclose a multiply accumulate unit instruction slot.

Moller discloses a multiply accumulate instruction unit (col 5 lines 11-12)

Sheaffer, a computer system that already contains an arithmetic logic unit, would likely be motivated to include instructions that provide further flexibility to the programmer. A multiply accumulate instruction is well known in the art and allows the programmer to complete varies applications in one instruction, rather than two—making

the system less complicated and often faster. For these reasons, Sheaffer would be motivated to include a multiply accumulate instruction.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the computing system of Sheaffer and include the multiply accumulate instruction/unit of Moller. Clearly, as this instruction is incorporated, instruction slots would be available to save a MAC instruction in instruction memory.

17. Regarding claim 11, Sheaffer/Miller/Moller discloses the memory system of claim 10 wherein the store unit instruction slot is an expanded width instruction slot that stores an expanded width store instruction including additional bits to extend compute register fiele addressing, an additional bit to extend address register file addressing (col 3 lines 16-19), an additional bit to expand an opcode file, or an additional bit to extend a conditional field.

Note that the "or clause" of the claim requires only one limitation to be anticipated.

18. Regarding claim 13, Sheaffer/Miller/Moller discloses the memory system of claim 10 where the load unit instruction slot is an expanded width instruction slot that stores an expanded width load instruction of a first format for load immediate operations including additional bits to extend compute register file addressing, a bit to extend address file register addressing (col 3 lines 16-19 and col 9 lines 13-19),

Note, in the second citation, that the result is stored in a double-wide register. Since this is treated as one register, this would suggest that loading would work the same way, extending the register addressing.

A bit to extend a conditional field or sixteen bits to extend an immediate field.

Note that, again, the "or clause" of the claim requires only one limitation to be anticipated.

19. Regarding claim 15, Sheaffer/Miller/Moller discloses the memory system of claim 10 where the ALU, MAU and DSU instruction slots are expanded width instruction slots that store expanded width ALUE, MAU, and DSU instructions including additional bits in each operand field to extend compute register file addressing (col 9 lines 13-19), a bit to extend an opcode field, or a bit to extend a data type field.

20. Claims 12, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheaffer/Miller/Moller in view of Tremblay (U.S. Patent No. 6,341,348).

21. Regarding claim 12, Sheaffer/Miller/Moller discloses the memory system of claim 11. wherein said expanded with store instruction supports expansion of a 32.times.32 bit/16.times.64 bit configurable register file size to a 128.times.32 bit/64.times.64 bit/32.times.128 bit configurable register file size.

Sheaffer/Moller fails to disclose a register file of size 128.times.32 bit/64.times.64 bit/32.times128 bit.

Tremblay discloses a register file with 128 32-bit registers (col 5 lines 39-41).

Sheaffer/ Moller fails to disclose the size of its register file. Sheaffer/Moller would likely be motivated to utilize a similar size as another VLIW invention (Tremblay col 5 line 57). Clearly, the size of the register file depends on particular aspects of the invention not necessarily disclosed in a patent attributed to a specific feature. Sheaffer/Miller/Moller would have been reasonably motivated to utilize a register file of any reasonable size.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the invention of Sheaffer/Miller/Moller and incorporate a register file with 128 32-bit registers. Sheaffer also discloses the technique of grouping registers into pairs and quads (col 1 line 66 to col 2 line 8), allowing for a register file with 64 64 bit registers and 32 128 bit registers.

22. Regarding claim 14, Sheaffer discloses the memory system of claim 13 wherein said expanded with load instruction supports expansion of a 32.times.32 bit/16.times.64 bit configurable register file size to a 128.times.32 bit/64.times.64 bit/32.times.128 bit configurable register file size (Tremblay col 5 lines 39-41 and Sheaffer col 1 line 66 to col 2 line 7--see claim 12).

23. Regarding claim 16, Sheaffer/Miller/Moller discloses the memory system of claim 15 wherein said expanded width ALU, MAU, and DSU instructions each supports expansion of a 32.times.32 bit/16.times.64 bit configurable register file size to a

128.times.32 bit/64.times.64 bit/32.times.128 bit configurable register file size (Tremblay col 5 lines 39-41 and Sheaffer col 1 line 66 to col 2 line 7--see claim 12).

24. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sheaffer/Miller in view of Pechanek (U.S. Patent No. 6,173,389).

25. Regarding claim 17, Sheaffer discloses a very long instruction word (VLIW) instruction (col 5 lines 48-51) memory (VIM) basket (VIMB) (col 7 lines 1-3)

an instruction bit organizer for receiving instructions as data and organizing the bits from the data encoded instructions into proper format for loading into the VIMB (see below);

And the VIMB comprising a plurality of instruction slots having expanded instruction slot width greater than the width of the instruction format required in program storage (col 1 lines 33-50 or col 2 line 65 to col 3 line 7).

Sheaffer/Miller fails to disclose a load indirect instruction or a mask bit field specifying which slots will be loaded in a VLIW having at least one instruction slot that is an expanded instruction slot, the VLIW accessible to be loaded at an addressable location into the VIMB.

Pechanek discloses a load indirect instruction and a load mask bit field (col 3 lines 24-33).

The technique in Pechanek is advantageous to utilize hardware more efficiently and reduce duplicate instructions (col 2 lines 12-27)

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Sheaffer/Miller and incorporate the indirect instruction with load mask bit field of Pechanek.

Response to Arguments

26. Applicant's arguments filed 28 April 2008 have been fully considered and some arguments were found persuasive.

27. Applicant argues that there are two instructions in Sheaffer rather than a single expanded instruction as required by the claims. In Examiner's opinion, the fact that Sheaffer has characterized this (these) instruction(s) as two separate instructions, rather than an extended instruction does not affect the validity of the rejection. Examiner has interpreted it to be a single extended instruction and this interpretation is well supported by the functionality of that instruction. Furthermore, col 1 lines 33-50 and col 2 line 65 to col 3 line 12 appear to characterize the NOP as a prefix or extension of that instruction.

However, on further inspection, it appears that Examiner's interpretation still fails to contain all limitations of the claimed invention. Firstly, Applicant's claims require a "VLIW memory having a plurality of instruction slots for storing VLIW instruction words." However, Sheaffer indicates that the instruction (as combined) becomes a VLIW instruction after the combination. This means, of course, that the instruction is not VLIW as stored in memory and Sheaffer alone fails to disclose a "VLIW memory having a

plurality of instruction slots for storing VLIW instruction words." Secondly, Applicant's claims require that "said plurality of instruction slots" (referring to the VLIW instruction slots) can contain "standard width instructions." Sheaffer contains standard width instructions, but fails to disclose standard with VLIW instructions, since the standard with instruction is not VLIW. These discrepancies between Sheaffer and the claimed invention are remedied in the obviousness type rejection presented in this Office Action.

28. Regarding claim 12, Applicant's claim discloses a 32x32 bit/ 16x64 bit configurable register file size to a 128x32 bit/64x64 bit/ 32x128 bit configurable register file size. Examiner asserts that the claim language was unclear whether (or how) the claim required a register size that is "to" a second register file size. Therefore, Examiner has interpreted the claim as requiring the larger size.

To that regard, Examiner combined the original reference with a further reference that included 128 32-bit registers. Examiner further notes that the primary reference discloses using those registers in pairs or quads. So, the 64x64 bit and 32x128 bit registers are also disclosed by this combination.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made.

The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183